Microtronix
Video LVDS Transmitter / Receiver

User Manual

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Document Revision History

This user guide provides basic information about using the Microtronix ***Video LVDS Transmitter / Receiver IP, PN: 6246-xx-xx***. The following table shows the document revision history.

Date	Description
April 2007	Initial Release – Version 1.0
September 2007	Minor updates – Version 1.1
November 2007	Minor updates – Version 1.2
January 2008	Added receive timing procedure – Version 1.3
March 2008	Added procedure to integrate the Core in a Quartus project – Version 1.4

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Typographic Conventions

Path/Filename	A path/filename
`[SOPC Builder]$ <cmd>`	A command that should be run from within the Cygwin Environment.
`Code`	Sample code.
↵	Indicates that there is no break between the current line and the next line.

Table of Contents

Features

- Optimized for video applications
- Single core supports LVDS transmitter and receiver functions
- Support for both 28-bit and 35-bit parallel data
- Supports 1, 2 and 4 link configurations
- No transmit PLL clock fine tuning required
- Support for OpenCore Plus evaluation
- Reference Designs

Introduction

The Microtronix ***Video LVDS SerDes Transmitter / Receiver IP-Core*** provides a complete, easy-to-use solution to interface with a wide variety of video host systems and flat panel displays.

The core simplifies the design of video LVDS interfaces, improves data integrity and timing margins. For example, the Transmitter has the unique ability to generate a LVDS transmit clock synchronous to the video data stream thereby eliminating the need to fine-tune a PLL to the outputted LVDS data. Similarly, the Receiver auto aligns the receive clock to the encoded video to assure data synchronization. An easy to use GUI enables the user to select the number of LVDS links and to configure the number data channels for each link.

The transmitter converts 28-bit parallel data into 4 LVDS data streams and one LVDS clock stream. The receiver converts 4 LVDS data streams into 28-bit parallel data. Adding a fifth channel increases the data width to 35 bits. Transmitter (and receiver) modules can be cascaded to create dual and quad LVDS links.

The Video LVDS SerDes Transmitter / Receiver core is optimized for Altera Cyclone II & Cyclone III family of programmable logic devices.

Transmitter

A block diagram of the Transmitter core is shown in Figure 1. The LVDS transmitter signals are listed in Table 1.

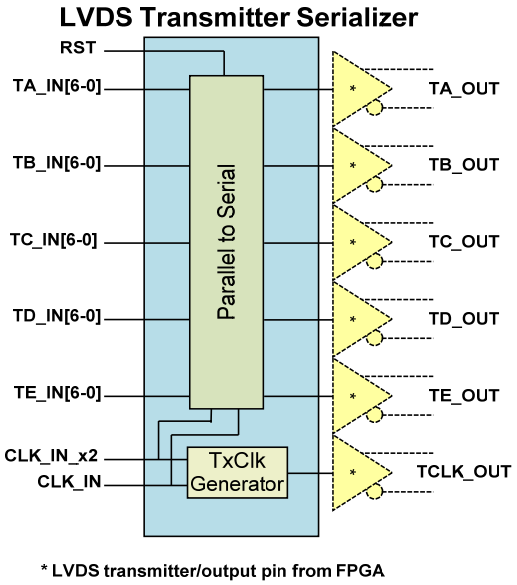


Figure 1: Block diagram of LVDS Transmit Serializer

Table 1: LVDS Transmitter signal assignments.

Signal	Direction	Description
RST	IN	Active high reset input
CLK_IN	IN	Clock input
CLK_IN_x2	IN	Clock input x7÷2
TA_IN[6-0]	IN	Channel A Parallel Data In
TB_IN[6-0]	IN	Channel B Parallel Data In
TC_IN[6-0]	IN	Channel C Parallel Data In
TD_IN[6-0]	IN	Channel D Parallel Data In
TE_IN[6-0]	IN	Channel E Parallel Data In
TA_OUT	OUT	LVDS Channel A Out
TB_OUT	OUT	LVDS Channel B Out
TC_OUT	OUT	LVDS Channel C Out
TD_OUT	OUT	LVDS Channel D Out
TE_OUT	OUT	LVDS Channel E Out
TCLK_OUT	OUT	LVDS Channel CLK Out

Receiver

A block diagram of the LVDS Receiver Deserializer core is shown in Figure 2. The LVDS Receiver signals are listed in Table 2.

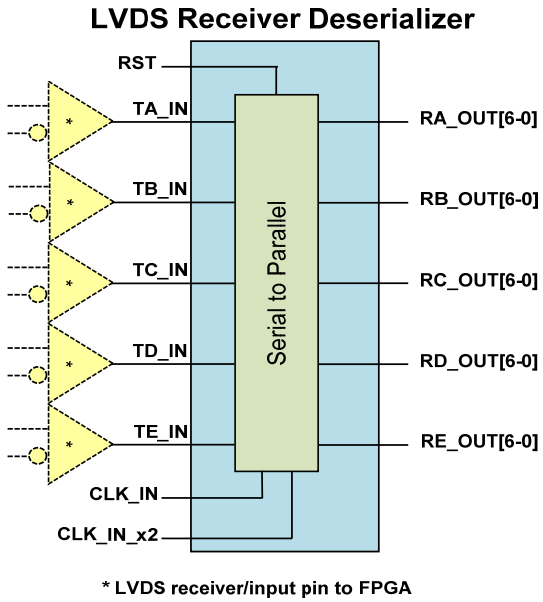


Figure 2: Black diagram of LVDS Receive Deserializer core

Table 2: LVDS Receiver signal assignments.

Signal	Direction	Description
RST	IN	Active high reset input
CLK_IN	IN	Clock input
CLK_IN_x2	IN	Clock input x7÷2
RA_IN	IN	LVDS Channel A In
RB_IN	IN	LVDS Channel B In
RC_IN	IN	LVDS Channel C In
RD_IN	IN	LVDS Channel D In
RE_IN	IN	LVDS Channel E In
RA_OUT[6-0]	OUT	Channel A Parallel Data Out
RB_OUT[6-0]	OUT	Channel B Parallel Data Out
RC_OUT[6-0]	OUT	Channel C Parallel Data Out
RD_OUT[6-0]	OUT	Channel D Parallel Data Out
RE_OUT[6-0]	OUT	Channel E Parallel Data Out

The LVDS Receiver clock input connects to a PLL that is used to generate CLK_IN and CLK_IN_x2 for the LVDS Deserializer. This PLL must be instantiated by the user (see Clock Generation).

Data Mapping

Figure 3 below shows the LVDS data mapping for the transmitter and receiver.

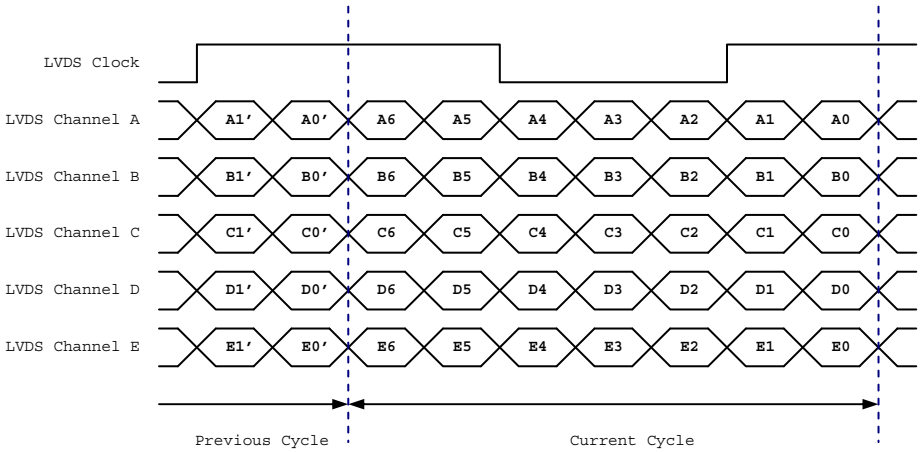


Figure 3: LVDS Mapping

Design Flow

The following steps describe how to integrate the LVDS SerDes Transmitter / Receiver IP core in a Quartus project.

- Open windows command prompt or Linux terminal window.
- Browse to the LVDS wizard directory <install_dir>/wizard.
- Start the wizard by typing java –jar mtx_lvds_gui.jar
- Alternatively, start the wizard from the Microtronix->HD Video LVDS Transmitter Receiver program group in the Start menu

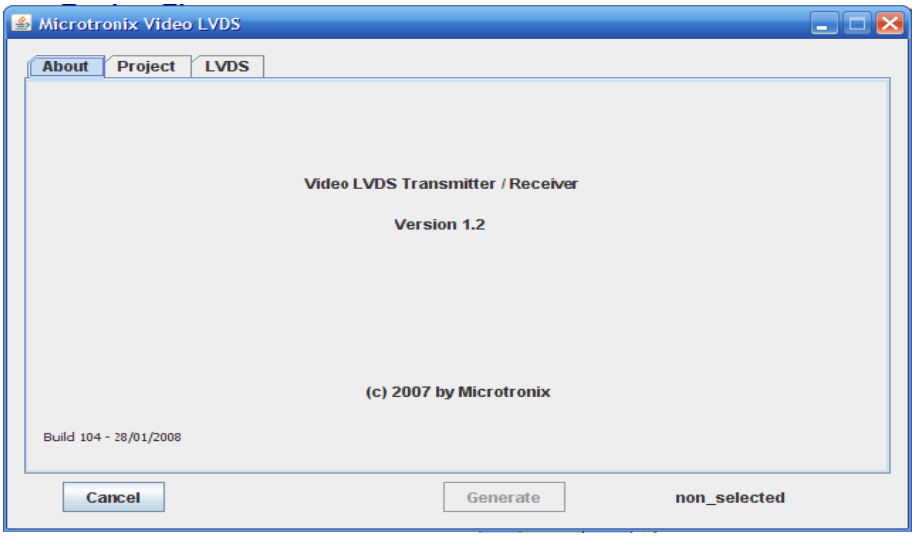


Figure 4: Wizard Overview

- Click on the Project tab.
- Use the browse button to select a new project or load an existing project.
- Select the appropriate FPGA device family (Cyclone II or Cyclone III) and speed grade.

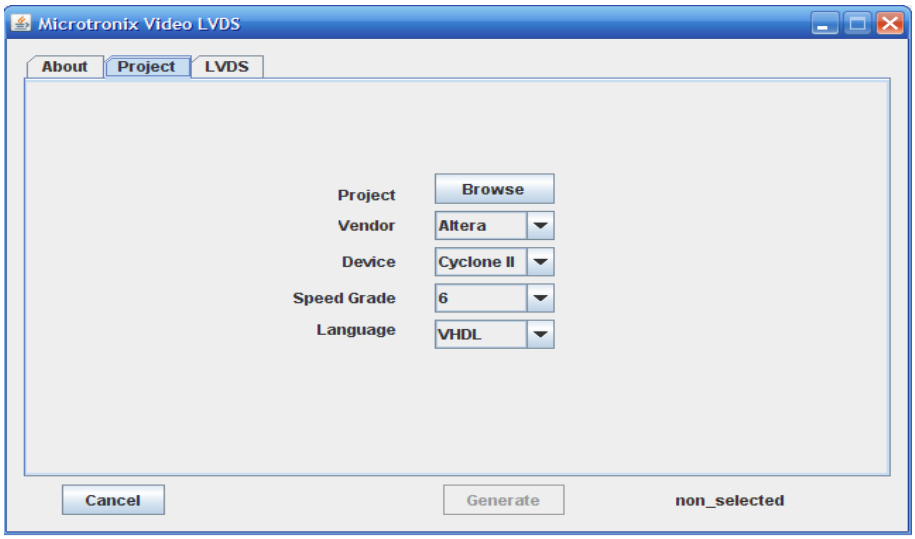


Figure 5: Project Tab

- Click on the LVDS tab to select the LVDS settings.
- Select the desired IP Architecture, either Transmitter or Receiver.
- Select the number of links and channels required by the design. Channel value represents the number of LVDS data streams and the Link value represents the number of groups of channels.

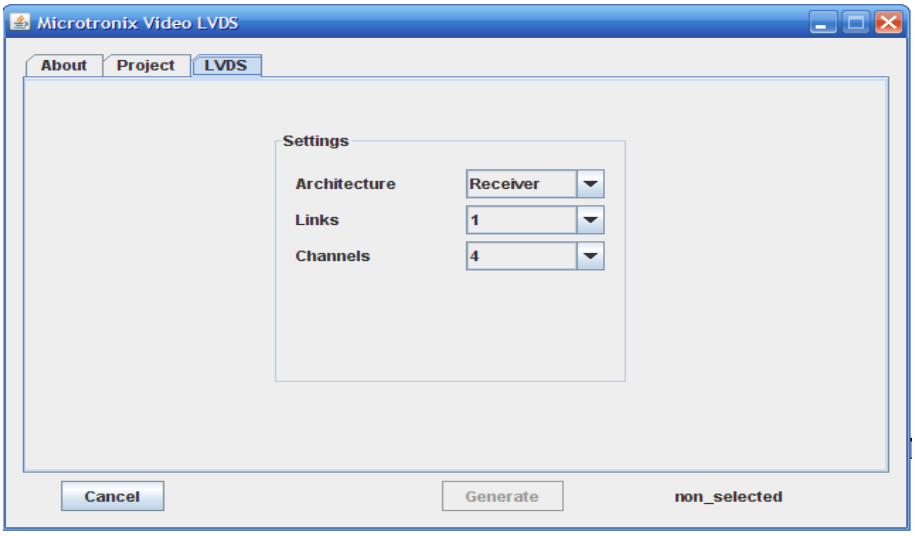


Figure 6: LVDS Tab

- Once all the appropriate options are selected, click on the Generate button to start the LVDS IP core generation.
- The wizard writes a top level LVDS entity.
- Start Quartus II and open the project.
- Add LVDS component to the project and connect the signals.
- Add the mtx_lvds_package to the project files (Assignments -> Settings -> Files). The mtx_lvds_package is located in the directory <install_dir>/synthesis.
- Add the directory <install_dir>/synthesis to the Quartus user libraries (Assignments -> Settings -> User Libraries).
- Start the compilation.

Clock Generation

A PLL is required to generate two clock inputs for the LVDS transmitter and receiver modules. The first PLL output connects to the CLK_IN clock. This clock has the same frequency as the PLL input clock. The second PLL output feeds the CLK_IN_x2 clock. This clock frequency is the PLL input clock multiplied by 7 and divided by 2. Select in the Quartus PLL MegaWizard that the second clock (c1) must be compensated.

On the Receiver side, the input to the PLL is the TCLK_OUT from the transmitter. The PLL input clock pin on the FPGA must be a dedicated clock (i.e. the general function of the pin must be that of a clock).

Figures 7 and 8 below show an example connection of both Transmitter and Receiver respectively.

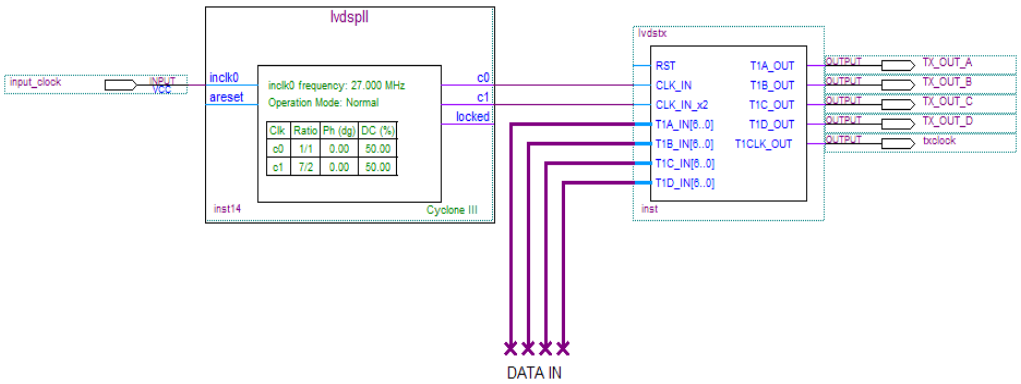


Figure 7: LVDS Transmitter

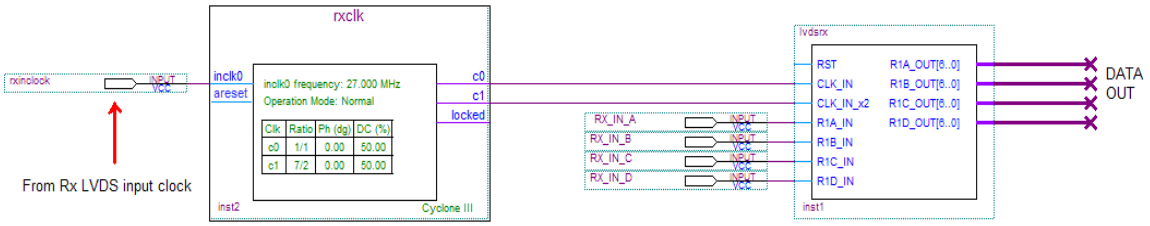


Figure 8: LVDS Receiver

When the PLL input clock is switched and the PLL loses lock, the PLL must be reset to maintain the phase relation between the PLL output clocks.

Assignments

Before starting the compilation in Quartus the I/O-standard for the LVDS receiver inputs and LVDS transmitter outputs must be set to LVDS.

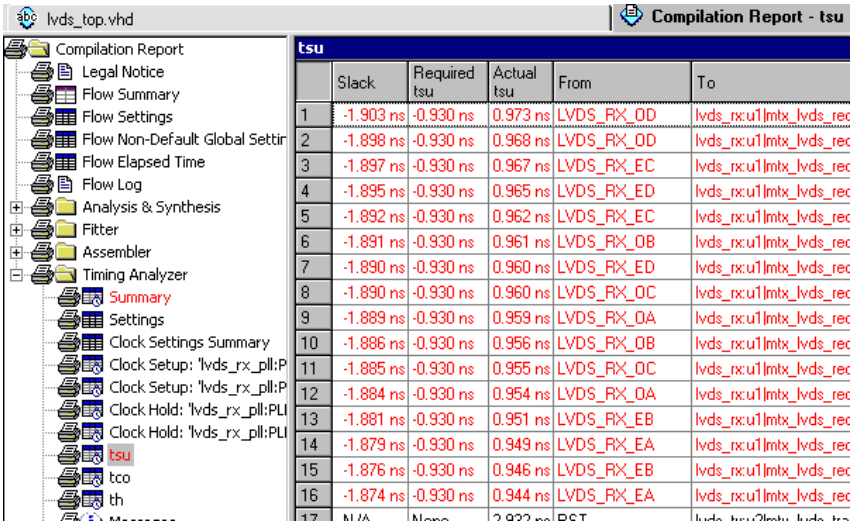
LVDS receiver inputs must have a setup time (tsu) requirement of negative one half of the LVDS bit time.

E.g. The LVDS receive clock is 74.25 MHz. The LVDS bit time is 1 / (74.25MHz * 7) = 1.92 ns. The setup time requirement is -962 ps.

It is helpful to add 20-30ps of margin to the setup time to avoid timing failures for paths that are slightly over the half bit time but still within an acceptable range. In the example below we will use –930 ps as our setup requirement.

Receive PLL Adjustment

To ensure that the received data bits are sampled correctly, the outputs of the receive PLL may need to be shifted. After the first Quartus compilation, look at the tsu (setup time) report under Timing Analyzer in the Compilation Report window.



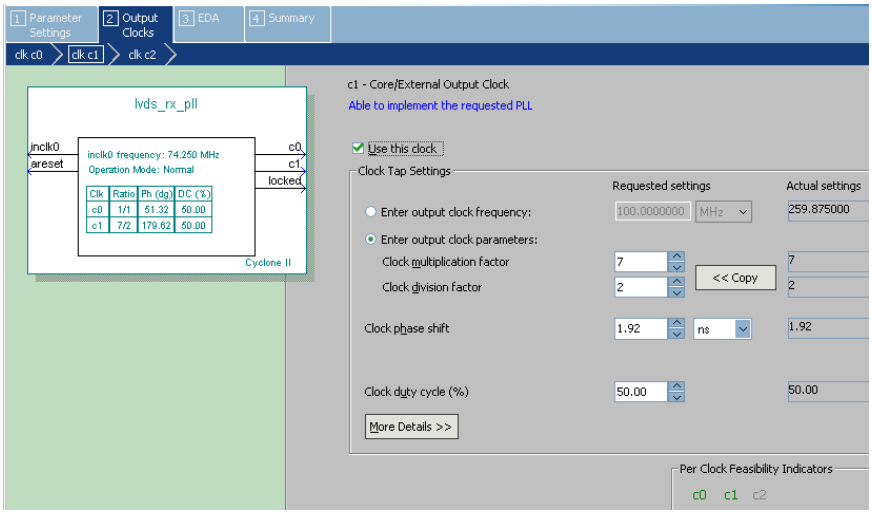
Take the maximum and minimum actual tsu values and average them to find the tsu midpoint. Subtract the desired tsu to determine the required PLL phase shift.

E.g. In the above image;

the midpoint = (0.973 + 0.944)/2 = 0.9585 ns,

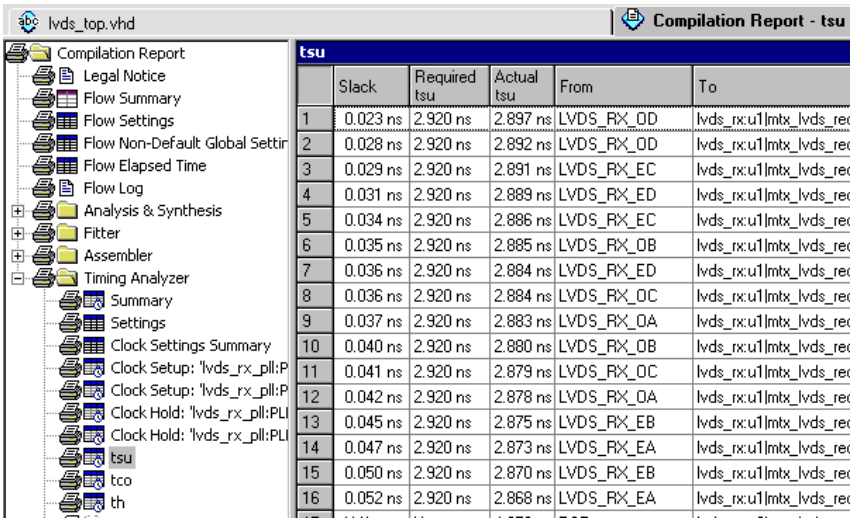
the phase shift = 0.9585 – (-0.962) = 1.92ns

Edit the receive PLL to add the output shift to both the single-rate clock and the 7/2 clock.



In cases where the PLL phase shift is close to or greater than an LVDS bit time, the Quartus timing analyzer will add one period of the 7/2 clock to the reported setup time. Adjust the tsu requirement by adding one period of the 7/2 clock.

E.g. –0.93ns + 1 / (7 * 74.25MHz / 2) = 2.92ns



Resource Requirements

Table 3 shows the typical size in logic elements (LE) for the various video LVDS modules. The actual number of logic elements may vary depending on the device family and Quartus settings.

Table 3: FPGA Resource requirements.

Module	LE
LVDS Transmitter	255
LVDS Receiver	260

Simulation

A precompiled simulation library is provided for performing simulations using ModelSim. The library is located in the <install_dir>/simulation directory. Perform the following steps to simulate your design with the video LVDS modules.

1. Launch ModelSim
2. Map the sdram memory controller library. At the ModelSim prompt type;
   vmap mtx_lvds <install_dir>/simulation/mtx_lvds

   If you use a newer version of ModelSim, you must refresh the precompiled library. At the Modelsim prompt type;
   vcom –refresh –work mtx_lvds
3. Compile all of the design files
4. Start the ModelSim simulation by typing;
   vsim –t ps –L mtx_lvds <top_level>

Verification

The video LVDS module has been verified on Microtronix Cyclone II & III development boards. Table 5 shows the hardware tested platforms and supported memory devices.

Development Board	Altera Device
ViClaro III	EP3C120F780C7
ViClaro II	EP2C35F484C6
ViClaro	EP2C20F256C7
Vivien	EP2C5T144C6

Table 5. Hardware Platforms

Installation

Follow these steps to install the Microtronix video LVDS modules on your computer.

1. Insert the Microtronix video LVDS modules Installation CD into your CD-ROM (or equivalent)
2. The setup program for the package should start. If it doesn't, browse to the CD using Windows Explorer and double-click on the setup icon.
3. Follow all the prompts. The setup program will attempt to auto-detect the installation location of the Quartus II. Please correct the specified paths if the setup program doesn't or incorrectly detects them.

License

A valid IP core license is required from Microtronix to generate program files incorporating the video LVDS IP-cores. These licenses are generated based on a NIC or Guard ID supplied by the user. They can be either server or workstation based.

After purchasing a license you receive your license file. Copy the license file (license.dat) to your current Quartus license file and the video LVDS (CC21_6246) will show in the Quartus License Setup (Tools->License Setup).

With the free OpenCore Plus feature the video LVDS can be evaluated in real hardware. An evaluation license from Microtronix is required for OpenCore Plus compilation.

Please contact Microtronix for licensing details.