



ViClaro III HD Video IP Development Kit

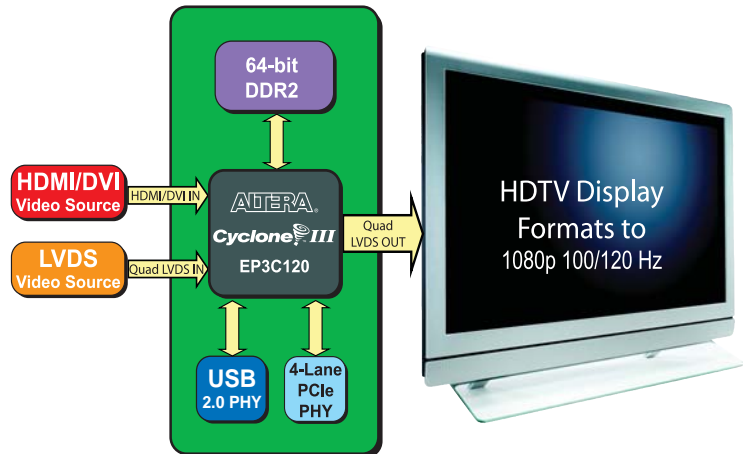
Product Brochure

Features

- Altera EP3C120 Cyclone™ III FPGA
- 256 MB 64-bit wide DDR2 memory
- 4-lane PCIe PHY
- 72 LVDS channels on Video Host Board
- Interfaces: LVDS, Mini-LVDS, RSDS & PPDS
- Quad Link LVDS Interface Card
- DVI or HDMI Receiver / Transmitter Card
- Altera compatible HSMC expansion connectors
- Suite of video reference designs

Includes the following IP Core licenses:

- Avalon Multi-port DDR2 Memory Controller IP Core
- Video LVDS SerDes Transmitter / Receiver IP Core
- I²C Master IP Core



Special Bonus Offer

Receive a FREE USB-Blaster Download Cable with your purchase of a ViClaro III HD Display Panel - Video IP Development Kit.

DESCRIPTION

The Microtronix ViClaro III HD Video IP Dev Kit is a versatile video and imaging processing IP development platform supporting all the interfaces for HD video display and imaging applications typically required by consumer, automotive and medical market segments.

Designed in conjunction with Altera®, the kit includes a suite of video processing IP reference examples, to provide a solid starting point for building your next generation HD 1080p 100/120 Hz video display product. The kit offers an unprecedented level of system integration to address the market needs for a flexible and powerful DVI, HDMI, SDI, HD/HDTV and PCIe engineering design-evaluation platform for the development of video processing IP algorithms.

The ViClaro III Dev Kit incorporates the latest Altera Cyclone III FPGA technology to enable you to build a highly integrated, low power, high performance and yet cost effective next generation HD video or LVDS panel display system. The kit includes the **Host Video board, a HSMC HDMI or DVI Receiver / Transmitter Board, Quad Link LVDS Interface daughter card and a Video LVDS Transmitter / Receiver IP Core**. The HSMC compatible expansion headers provide the versatility for custom add-on boards.

Video Reference Designs & IP Cores

The video reference designs are based on *Altera's Avalon-ST® VIP system interconnected framework* which simplifies the development of HD video processing systems. The kit includes a fully licensed copy of the Microtronix LVDS SerDes Transmitter core, Cyclone III Multi-port DDR2 cores and the I²C Master IP core.

The PCI Express reference designs incorporate a 4-lane PCIe IP core from Northwest Logics Inc. The user is required to license this IP core if they are to build custom designs incorporating PCIe functionality. Linux drivers are supplied supporting read/write access to on-board devices and for building streaming video applications.

ViClaro III HD Video Host Board

The ViClaro III HD Video Host Board contains the Cyclone III FPGA, USB 2.0 PHY, 4 lane PCIe PHY (note 1), DDR2 memory, two HSMC connectors and one dedicated HSMC LVDS connector for adding an application specific daughter card. The HSMC connectors are compliant with the Altera HSMC specification. The card supports a total of 72 LVDS channels.

The board supports a serial EEPROM with SHA-1 engine to provide protection of FPGA IP cores using signature device authentication.

Quad Link LVDS Interface Card

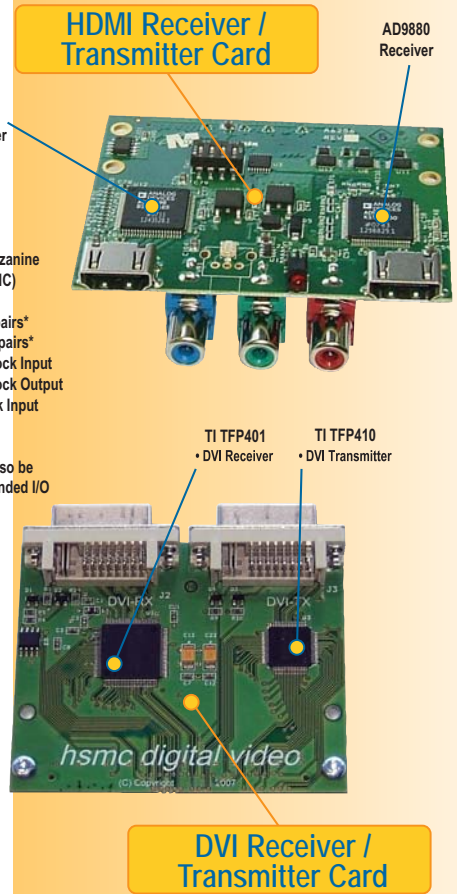
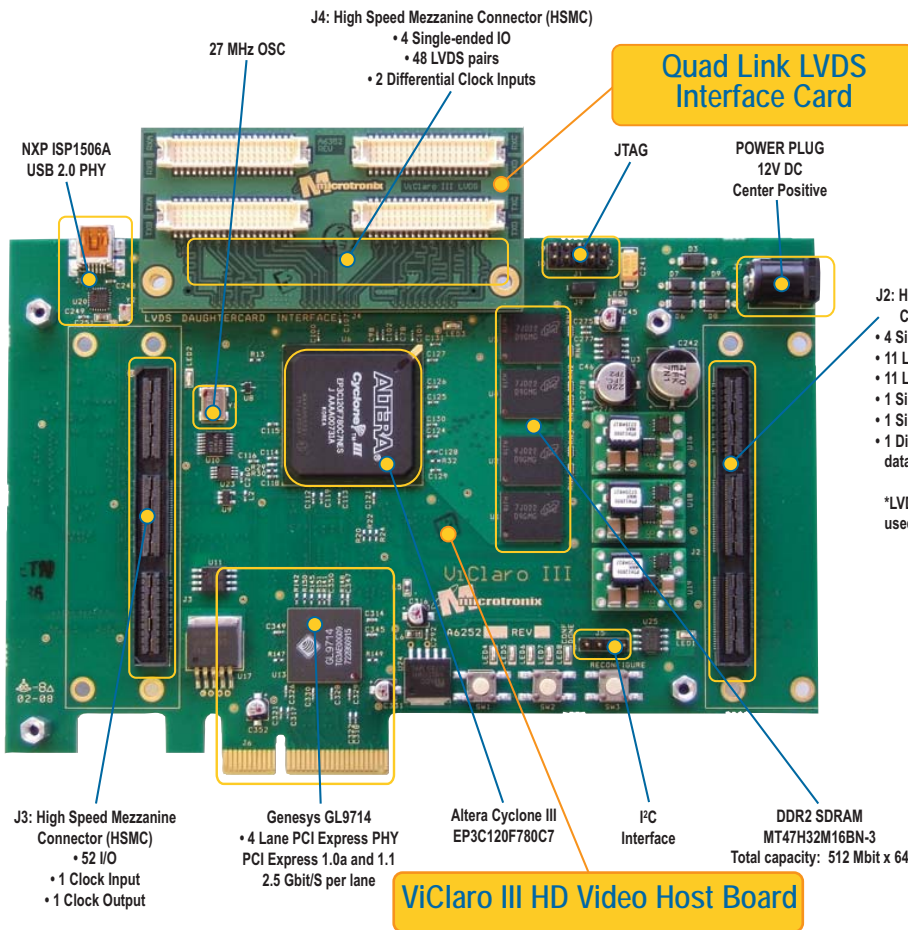
The **Quad Link LVDS Interface Card** supports 4 LVDS receive and transmit links each consisting of 5 data channels and 1 clock for a total of 48 LVDS pairs. The standard configuration of 20 Tx + 4 clk and 20 Rx + 2 clk, is capable of supporting LCD display panels up to 1080p at 100/120Hz. On-board LVDS termination resistors can be removed to convert receiver channels into transmitters as required to support 12 or 14-bit color applications.

The card is designed to support a broad range of LCD panels using LVDS, Mini-LVDS, RSDS, and PPDS low-voltage panel interface signalling. Custom LVDS daughter cards supporting alternative panel interface headers can be designed to meet your custom requirements.

DVI and HDMI HSMC Receiver / Transmitter Cards

The ViClaro is supplied with either a DVI or HDMI Receiver / Transmitter HSMC Daughter Card capable of supporting display resolutions from VGA to UXGA (1600x1200 and 1920x1080 [1080p@60]).

The **DVI Receiver / Transmitter Card** integrates a DVI 1.0 receiver and transmitter onto a single card. The **HDMI Receiver / Transmitter Card** provides an HDMI 1.2 receiver, a HDMI 1.2 transmitter and an analog YCrCb video receiver. The cards are supplied with source code examples and support for programming EDID data.



***Supplied Quartus Reference Designs**

- Quad LVDS links driving 1080p 100/120 Hz display panel
- Looped DVI-DVI video at 720p/1080i/1080p
- Looped DVI-LVDS HD video
- Looped LVDS-LVDS HD video
- Video capture at 720p/1080i/1080p
- Picture-in-Picture (PIP)
- 1080i-50 Input - VIP de-interlacer
- 720p to 1080p video scaling

Kit Contents Include:

- ViClaro III HD Video Host Board
- Quad Link LVDS Interface Card
- DVI or HDMI Receiver / Transmitter Card
- Video LVDS SerDes Tx / Rx IP Core
- 12VDC-120/240VAC power adapter
- 2 – LVDS Loopback Cables
- CD with Reference Designs, Linux drivers & Documentation

*Release for Quartus 8.0 will have slightly different designs. Please contact sales for details.

Design Security

An on-board EEPROM can be used to generate encryption keys at start-up for validation of the IP cores and prevent unauthorized copying of proprietary IP technology.

ORDERING INFORMATION

PART NUMBER	DESCRIPTION
6252-01-01	ViClaro III HD Video IP Dev. Kit with DVI
6252-02-01	ViClaro III HD Video IP Dev. Kit with HDMI

*HDCP License is not included. Please contact sales for details.

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