

Microtronix Firefly Module

Revision B
Datasheet



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This datasheet provides information regarding the Product Starter Kit. The following table shows the document revision history.

Document Revision History	
Date	Description
May 2005	Initial Release – Version 1.0

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Typographic Conventions

Path/Filename	A path/filename
[SOPC Builder]\$ <cmd>	A command that should be run from within the Cygwin Environment.
...sdk/<path>	A file that is relative to the sdk directory.
Code	Sample code.
↵	Indicates that there is no break between the current line and the next line.

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Features

Firefly Module

- Altera EP1C12F324C8 or EP1C4F324C8 Cyclone FPGA
- Altera EPCS4 or EPCS1 Active Serial Configuration Device
- Supports Nios II soft core processor
- Supports self-reconfiguration of FPGA from logic in FPGA
- On-board 24MHz oscillator
- 8 Mb Flash (one 8M x 16-bit chip)
- 16 Mb SDRAM (PC-133 compatible, one 4M x 32-bit chip)
- RS-232 Transceiver (2 receive, 2 transmit)

General Description

The Firefly Module is intended to provide a drop-in uClinux system for embedded systems. It provides a Cyclone FPGA for a Nios II soft-core processor as well as enough SDRAM and Flash to run the uClinux operating system. A large I/O count allows the module to be used in many diverse applications. Communication and programming is provided through Altera's standard utilities.

Board Components

This section describes the various components and sub-circuits of the Microtronix Firefly Module. For each component or circuit, this section explains: basic function, performance limits, I/O requirements, and how to interface to the Avalon Bus in a Nios II based system (including custom interface components). Figure 1 shows the location of all the Product Starter Kit components mentioned in this section.

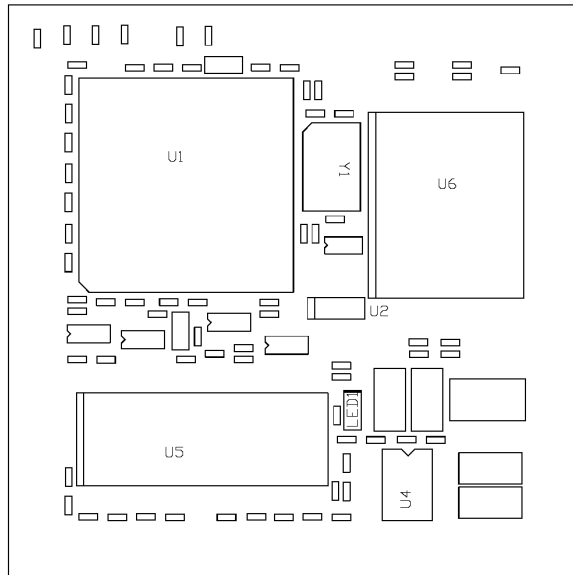


Figure 1: Firefly Components

Cyclone FPGA

U1 in Figure 1 is an Altera Cyclone EP1C12F324C8 or EP1C4F324C8 FPGA device in a 324 pin FineLine BGA® package. Table 1 lists the Cyclone device features.

Table 1: Cyclone Device Features

	EP1C12F324C8	EP1C4F324C8
LEs	12,060	4,000
M4K RAM Blocks	52	17
Total RAM Bits	239,616	78,336
PLLs	2	2
Maximum User I/Os	249	249
Maximum Clock Speed	275MHz	275MHz

Active Serial Configuration Device

U2 in Figure 1 is an Active Serial Configuration Device EPCS4 (for the 1C12 module) or EPCS1 (for the 1C4 module). This device is a serial flash device with additional state machine logic for handshaking with the Active Serial Programming feature of the Cyclone FPGA. After a Power-On or Reconfig event, the Cyclone FPGA and Active Serial Programming Device work together to load a design from the flash memory of the configuration device into Cyclone FPGA SRAM cells. Once configuration is complete, the new core starts running.

Detailed information about the configuration device, as well as design file sizes, can be found in Table 2 below.

Table 2: Active Serial Configuration Devices

	EPCS4	EPCS1
Flash Memory Size (bits)	4,194,304	1,048,576
Max Serial Clock Frequency	20MHz	20MHz
Max Uncompressed Design Size (bits)	2,326,528	924,512
Min area left for general use (bits)	1,867,776	124,064
Compression Performance	35-60%	35-60%
Power On Reset Time	100ms	100ms

The minimum area left for general use in the flash memory of the configuration device can be used by software running on a soft-core processor in the Cyclone FPGA (such as an Altera Nios II) to store configuration information, programs, other compressed core designs, etc. If an Altera Nios II based system is running on the FPGA, the EPCS Serial Flash Controller SOPC component, along with software routines provided by the HAL can be used to access the portions of EPCS flash memory that are not being used to hold the core design.

The Active Serial Programming Device also supports compression of the designs being held within it. The compression is enabled from the Quartus II design tool when compiling a logic design. The Active Serial Programming Device will send a compressed data bit stream to the Cyclone FPGA, which will decompress the data locally in real time and use the uncompressed data to program its SRAM based logic cells.

See the Altera configuration literature page for EPCS related documentation at <http://www.altera.com/literature/lit-config.jsp>.

Flash

U6 in Figure 1 is a 8MB FLASH chip (4M x 16-bit) chip with a 120ns access time. The FLASH sits on its own 16-bit dedicated bus.

Interfacing the FLASH with a SOPC based system can be easily accomplished using the “Flash Memory (Common Flash Interface)” SOPC component available that comes with Altera’s Nios II distribution. For proper operation, use the following parameters with the SOPC component: address width 22 bits, data width 16 bits, setup 20ns, wait 100ns, hold 45ns. This component also requires it’s own “Avalon Tri-State Bridge” to connect to the CPU. See n2cpu_nii51013.pdf in the Nios II documents subdirectory for further details.

Included in the Firefly package are two SOPC board components describing the two variations of the Firefly module. By selecting the Microtronix Firefly (1C12 or 1C4 as appropriate) as the target board, the flash can be programmed using Altera’s Nios II flash programmer tool.

SDRAM

U5 in Figure 1 is a 16Mbyte SDRAM chip (4M x 32-bit) chip with a 7ns access time (PC133 compatible SDR SDRAM). The SDRAM exists as a 32-bit wide device on its own dedicated bus.

Interfacing the SDRAM with a SOPC based system can be easily accomplished using the Altera SDRAM SOPC component (see n2cpu_nii51005.pdf in the Nios II documents subdirectory for further details). The SDRAM chip used on the µKit board is available pre-defined in the SDRAM SOPC component. Choose “single Micron MT48LC4M32B2-7 chip” from the “Presets:” list.

Along with the SOPC builder component, the SDRAM requires a clock signal. This signal should be provided by a PLL megafunction in Quartus II. Pin J3 should be used as the input clock (24MHz on-module oscillator) and pin K4 should be used as the output to the SDRAM. The frequency of the output should match the frequency of the SOPC Builder system.

RS-232

U4 in Figure 1 is a Maxim Semiconductor 4-wire UART transceiver (2 input, 2 output) part MAX3232, capable of 115,200 baud transfer rate (max).

Interfacing the UART transceiver with a SOPC based system can be easily accomplished using the Altera UART SOPC component. See n2cpu_nii51010.pdf in the Nios II documents subdirectory for further details.

Clock

Y1 in Figure 1 is a 24MHz oscillator. It is connected to the Cyclone PLL 1 through pin J3. The external output of this PLL is pin K4 that is connected to the clock of the SDRAM device.

Module Connector

Around the bottom of the module is a double row of 0.1" (2.54mm) pitch pins. The recommended connectors for mating with the Firefly are Samtec's SSW series. Four dual-row 36-pin sockets are required (SSW-118-21-G-D).

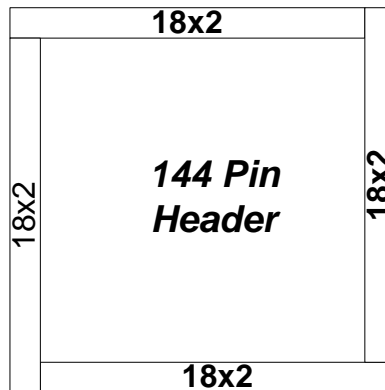


Figure 2: Firefly Connector

External Support Circuitry

This section describes the support circuitry required by the Firefly Module.

Power Supply

Two different voltages are required to power the Firefly Module. Peripherals and Cyclone I/O require 3.3V while the Cyclone core requires 1.5V.

Due to the nature of FPGA technology, their power requirements vary greatly depending on how they are configured. Fortunately, Altera provides a tool for estimating Cyclone power requirements. It can be found on the Altera web site at

<http://www.altera.com/support/devices/estimator/pow-powerplay.html>.

Power calculations for the 3.3V supply must take into account the power requirements of the Firefly on-board peripherals (SDRAM, Flash, etc). The maximum current requirement for all 3.3V devices (excluding the Cyclone) is 500mA.

The Firefly is targeted at Nios II based FPGA designs. For such applications, the recommended power supplies are shown in Table 3. These values are sufficient to power Nios II based Firefly designs.

Table 3: Recommended Supply Current, Nios II Based Application

Voltage	Current
3.3V	1 A
1.5V	1 A

A number of companies provide resources specifically targeted at designing power supplies for Altera FPGAs. Two such companies are Linear Technologies (<http://www.linear.com/designtools/Altera.jsp>) and Texas Instruments (<http://www.ti.com/alterafpga>).

JTAG

A 10-pin, dual-row, 0.1" (2.54mm) pitch header is required for JTAG programming and communication. Figure 3 shows the connections required to support Altera JTAG programming hardware.

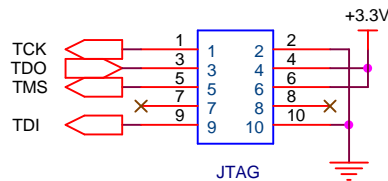


Figure 3: JTAG Circuitry

Active Serial

The Firefly module allows for direct access to the EPCS1 or EPCS4 serial configuration device. A 10-pin, dual-row, 0.1" (2.54mm) pitch header is required for programming this device. Figure 4 shows the connections required to support Altera active serial programming hardware.

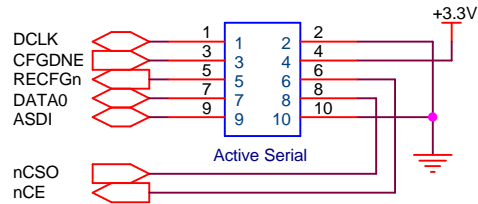


Figure 4: Active Serial Circuitry

Appendix A: Cyclone FPGA Pinouts

The following table lists all of the pin connections to the Cyclone device from the components on the Firefly Module.

Pin #	Signal	Connected to...	Comments	
R9	FLASH_A0	FLASH (U6) Address		
V10	FLASH_A1			
U10	FLASH_A2			
T10	FLASH_A3			
R8	FLASH_A4			
V9	FLASH_A5			
U9	FLASH_A6			
T9	FLASH_A7			
R5	FLASH_A8			
V6	FLASH_A9			
U6	FLASH_A10			
T6	FLASH_A11			
V4	FLASH_A12			
U5	FLASH_A13			
T5	FLASH_A14			
U4	FLASH_A15			
U16	FLASH_A16			
R7	FLASH_A17			
V8	FLASH_A18			
U8	FLASH_A19			
U7	FLASH_A20			
T7	FLASH_A21			
U3	FLASH_A22	FLASH (U6) Address	Used for optional 16 and 32 MB FLASH	
R4	FLASH_A23	FLASH (U6) Address	Used for optional 16MB FLASH	
V11	FLASH_DQ0	FLASH (U6) Data (16-bit)		
T12	FLASH_DQ1			
V12	FLASH_DQ2			
T13	FLASH_DQ3			
V13	FLASH_DQ4			
R14	FLASH_DQ5			
R13	FLASH_DQ6			
U15	FLASH_DQ7			
R10	FLASH_DQ8			
U12	FLASH_DQ9			
R11	FLASH_DQ10			
U13	FLASH_DQ11			
R12	FLASH_DQ12			
T14	FLASH_DQ13			
T15	FLASH_DQ14			
V15	FLASH_DQ15			
U11	FLASH_OEn	FLASH (U6) Control		
V7	FLASH_WEn			
T11	FLASH_CEn			
T8	FLASH_ACC			FLASH_ACC should be tied to ground for normal operation
T4	FLASH_WPn			FLASH_WPn must be high to enable writing to the FLASH. A low signal will enable write-protect.
R6	FLASH_RSTn			

Pin #	Signal	Connected to...	Comments
E10	RECONFIGn	CONFIGURATION CIRCUIT	<p> Toggling this line will force the Cyclone FPGA to reconfigure itself using the Data in the Active Serial Configuration Device (U15) </p>
M4	SDRAM_A0	SDRAM (U5) <i>Address</i>	
M5	SDRAM_A1		
M6	SDRAM_A2		
L3	SDRAM_A3		
L2	SDRAM_A4		
H1	SDRAM_A5		
H2	SDRAM_A6		
H3	SDRAM_A7		
G3	SDRAM_A8		
G2	SDRAM_A9		
L4	SDRAM_A10		
L7	SDRAM_A11	SDRAM (U5) <i>Data (32-bit)</i>	
D4	SDRAM_DQ0		
E4	SDRAM_DQ1		
E5	SDRAM_DQ2		
F4	SDRAM_DQ3		
F5	SDRAM_DQ4		
F6	SDRAM_DQ5		
G4	SDRAM_DQ6		
G5	SDRAM_DQ7		
F2	SDRAM_DQ8		
F3	SDRAM_DQ9		
E3	SDRAM_DQ10		
E2	SDRAM_DQ11		
D1	SDRAM_DQ12		
D2	SDRAM_DQ13		
D3	SDRAM_DQ14		
C2	SDRAM_DQ15		
N6	SDRAM_DQ16		
N5	SDRAM_DQ17		
N4	SDRAM_DQ18		
N3	SDRAM_DQ19		
P4	SDRAM_DQ20		
P3	SDRAM_DQ21		
R3	SDRAM_DQ22		
T3	SDRAM_DQ23		
T2	SDRAM_DQ24		
R2	SDRAM_DQ25		
R1	SDRAM_DQ26		
P2	SDRAM_DQ27		
N2	SDRAM_DQ28		
N1	SDRAM_DQ29		
M1	SDRAM_DQ30		
M2	SDRAM_DQ31	SDRAM (U5) <i>Byte Enables</i>	
F7	SDRAM_DQM0		
F1	SDRAM_DQM1		
N7	SDRAM_DQM2	SDRAM (U5) <i>Bank Address</i>	
M3	SDRAM_DQM3		
L6	SDRAM_BA0	SDRAM (U5) <i>Control</i>	
L5	SDRAM_BA1		
H5	SDRAM_RASn		
H6	SDRAM_CASn		
G6	SDRAM_WEn		
H4	SDRAM_CSn	SDRAM (U5) <i>Clock</i>	
G1	SDRAM_CKE		
K4	SDRAM_CLK		

Pin #	Signal	Connected to...	Comments
P10	RS232_TXD	RS-232 (U4, P1)	
P9	RS232_RXD		
P12	RS232_CTS		
P13	RS232_RTS		
J3	FPGA_PLL_IN_A	Oscillator (Y1)	24 MHz

The following table lists all of the pin connections to the Cyclone device from the external pins of the Firefly Module.

Cyclone Pin #	Firefly Pin	Signal	Connected to...
F18	C1	EPM_A0	FPGA (U2)
D18	D1	EPM_A1	
C17	E1	EPM_A2	
D16	F1	EPM_A3	
D15	G1	EPM_A4	
E15	K1	EPM_A5	
G16	W2	EPM_A6	
F15	H2	EPM_A7	
E14	P1	EPM_A8	
G14	T1	EPM_A9	
G13	U1	EPM_A10	
F12	V1	EPM_A11	
G12	X1	EPM_A12	
L18	B9	EPM_A13	
H18	B2	EPM_A14	
G18	C2	EPM_A15	
F17	D2	EPM_A16	
D17	F2	EPM_A17	
E16	L1	EPM_A18	
G17	N1	EPM_A19	
F16	K2	EPM_A20	
H17	L2	EPM_A21	
H16	N2	EPM_A22	
G15	P2	EPM_A23	
F14	R2	EPM_A24	
H15	T2	EPM_A25	
H14	U2	EPM_A26	
E17	G2	EPM_A27	
H13	X2	EPM_A28	
J13	Y2	EPM_A29	
L17	A9	EPM_B0	FPGA (U2)
M18	A10	EPM_B1	
N17	A12	EPM_B2	
N18	A13	EPM_B3	
R16	A15	EPM_B4	
R18	A16	EPM_B5	
T16	A17	EPM_B6	
L16	B8	EPM_B7	
M16	A2	EPM_B8	
M17	B10	EPM_B9	
N16	B12	EPM_B10	
P17	B13	EPM_B11	
P16	B14	EPM_B12	
R15	B15	EPM_B13	
R17	B16	EPM_B14	
T17	B18	EPM_B15	

Cyclone Pin #	Firefly Pin	Signal	Connected to...
L15	A19	EPM_C0	FPGA (U2)
M15	B19	EPM_C1	
L14	C19	EPM_C2	
N14	E19	EPM_C3	
L13	F19	EPM_C4	
N13	G19	EPM_C5	
D12	H19	EPM_C6	
D11	K19	EPM_C7	
D10	M19	EPM_C8	
D8	N19	EPM_C9	
D7	P19	EPM_C10	
N15	B20	EPM_C11	
P15	D20	EPM_C12	
P14	E20	EPM_C13	
M13	F20	EPM_C14	
E13	H20	EPM_C15	
E11	K20	EPM_C16	
D9	M20	EPM_C17	
E8	N20	EPM_C18	
E7	R20	EPM_C19	
E6	T20	EPM_C20	
B14	Y4	EPM_D0	FPGA (U2)
B10	Y5	EPM_D1	
A10	Y6	EPM_D2	
B7	Y8	EPM_D3	
B9	Y9	EPM_D4	
B6	Y11	EPM_D5	
C6	Y12	EPM_D6	
A6	Y14	EPM_D7	
B4	Y15	EPM_D8	
B5	Y16	EPM_D9	
C11	X3	EPM_D10	
C10	X5	EPM_D11	
A9	X6	EPM_D12	
C9	X7	EPM_D13	
A8	X8	EPM_D14	
C7	X9	EPM_D15	
A7	X11	EPM_D16	
B8	X12	EPM_D17	
C8	X13	EPM_D18	
A4	X14	EPM_D19	
C5	X15	EPM_D20	
J15	A7	CLK_IN+	FPGA (U2) PLL2
J16	B7	CLK_IN-	
K15	A6	CLK_OUT+	
K16	B6	CLK_OUT-	
P10	Y17	TXD	RS-232 (U4)
P9	Y18	RXD	
P12	X18	CTS	
P13	X17	RTS	

Appendix B: Firefly Module Pin Diagram

